L Number	Hits	Search Text	DB	Time stamp
1	9157	(stress adj2 test\$3) or (burn-in adj2 test\$3)	USPAT; EPO; JPO;	2004/01/15 11:23
2	1019	((stress adj2 test\$3) or (burn-in adj2 test\$3)) near5 (IC or (integrated adj2	DERWENT USPAT; EPO; JPO;	2004/01/15
3	1154	<pre>circuit\$1)) ((stress adj2 test\$3) or (burn-in adj2</pre>	DERWENT USPAT;	2004/01/15
	0.70	test\$3)) near10 (IC or (integrated adj2 circuit\$1))	EPO; JPO; DERWENT	10:03
4	830	((stress adj2 test\$3) or (burn-in adj2 test\$3)) near3 (IC or (integrated adj2 circuit\$1))	USPAT; EPO; JPO; DERWENT	2004/01/15
5	149	(((stress adj2 test\$3) or (burn-in adj2 test\$3)) near3 (IC or (integrated adj2	USPAT; EPO; JPO;	2004/01/15 10:24
6	418	circuit\$1))) and (latch\$2 or flip-flop\$1) (((stress adj2 test\$3) or (burn-in adj2 test\$3)) near3 (IC or (integrated adj2	DERWENT USPAT; EPO; JPO;	2004/01/15 10:25
7	12	circuit\$1))) and (plurality or multiple near3 (latch\$2 or flip-flop\$1)) (((stress adj2 test\$3) or (burn-in adj2	USPAT;	2004/01/15
		<pre>test\$3)) near3 (IC or (integrated adj2 circuit\$1))) and ((plurality or multiple) near3 (latch\$2 or flip-flop\$1))</pre>	EPO; JPO; DERWENT	10:29
8	121	<pre>(stress\$3 near3 (IC or (integrated adj2 circuit\$1))) and (latch\$2 or flip-flop\$1)</pre>	USPAT; EPO; JPO; DERWENT	2004/01/15
9	83	(stress\$3 adj3 (IC or (integrated adj2 circuit\$1))) and (latch\$2 or flip-flop\$1)	USPAT; EPO; JPO; DERWENT	2004/01/15
10	15	<pre>(stress\$3 adj3 (IC or (integrated adj2 circuit\$1))) same (latch\$2 or flip-flop\$1)</pre>	USPAT; EPO; JPO; DERWENT	2004/01/15 10:32
11	15	<pre>(stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) same (latch\$2 or flip-flop\$1)</pre>	USPAT; EPO; JPO; DERWENT	2004/01/15 10:33
12	0	(stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and LSSD	USPAT; EPO; JPO; DERWENT	2004/01/15
13	0	(stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and ((scan adj2 design\$1) or	USPAT; EPO; JPO;	2004/01/15 10:36
16	0	LSSD) (stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and (714/726.ccls.)	DERWENT USPAT; EPO; JPO;	2004/01/15
17	0	(stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and (714/727.ccls.)	DERWENT USPAT; EPO; JPO;	2004/01/15
14	3	(stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and ((scan adj2 test\$3) or	DERWENT USPAT; EPO; JPO;	2004/01/15 10:38
15	5	LSSD) (stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and (714/724.ccls.)	DERWENT USPAT; EPO; JPO;	2004/01/15 11:06
18	0	(stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and (714/!.ccls.)	DERWENT USPAT; EPO; JPO;	2004/01/15 11:07
19	21	((stress adj2 test\$3) or (burn-in adj2 test\$3)) and LSSD	DERWENT USPAT; EPO; JPO;	2004/01/15 13:12
20	972		DERWENT USPAT; EPO; JPO;	2004/01/15 13:13
21	20	(reduc\$4 near5 current) near10 ((stress or burn-in) adj4 test\$3)	DERWENT USPAT; EPO; JPO;	2004/01/15 13:14
22	52	(reduc\$4 near5 current) same ((stress or burn-in) adj4 test\$3)	DERWENT USPAT; EPO; JPO;	2004/01/15
			DERWENT	

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23	1279	((stress or burn-in or accelerat\$4) adj4	USPAT;	2004/01/15
23	12.5	test\$3) near10 ((integrated adj2 circuit)	EPO; JPO;	13:28
		or IC\$2)	DERWENT	
24	956	((stress or burn-in or accelerat\$4) adj2	USPAT;	2004/01/15
		test\$3) near4 ((integrated adj2 circuit)	EPO; JPO;	13:50
25	0.00	or IC\$2)	DERWENT	2004/01/15
25	869	((stress or burn-in) adj2 test\$3) near4 ((integrated adj2 circuit) or IC\$2)	USPAT; EPO; JPO;	13:50
		(\integrated adjz critary or icaz)	DERWENT	1 13.30
26	1	(((stress or burn-in) adj2 test\$3) near4	USPAT;	2004/01/15
	_	((integrated adj2 circuit) or IC\$2)) same	EPO; JPO;	13:51
		(reduc\$5 near3 current)	DERWENT	
27	27		USPAT;	2004/01/15
		((integrated adj2 circuit) or IC\$2)) and (reduc\$5 near3 current)	EPO; JPO; DERWENT	13:58
28	4	·	USPAT;	2004/01/15
20	3	adj2 circuit) or IC\$2)) and (reduc\$5	EPO; JPO;	14:00
1		near3 current)	DERWENT	
29	35	(test\$3 near2 ((integrated adj1 circuit)	USPAT;	2004/01/15
		or IC\$2)) same (reduc\$5 near3 current)	EPO; JPO;	14:01
			DERWENT	0004/01/15
30	421	(test\$3 near2 ((integrated adj1 circuit)	USPAT;	2004/01/15 14:01
		or IC\$2)) and (reduc\$5 near3 current)	EPO; JPO; DERWENT	14:01
31	75	(test\$3 near2 ((integrated adj1 circuit)	USPAT:	2004/01/15
	'*	or IC\$2)) and (reduc\$5 near3 current) and	EPO; JPO;	14:02
		flip-flop\$1	DERWENT	
32	163		USPAT;	2004/01/15
		or IC\$2)) and (reduc\$5 near3 current) and	EPO; JPO;	14:02
		(flip-flop\$1 or latch\$3)	DERWENT	2004/01/15
33	23	(test\$3 near2 ((integrated adj1 circuit) or IC\$2)) and (reduc\$5 near3 current) and	USPAT; EPO; JPO;	2004/01/15 14:03
		((plurality or multiple) adj3	DERWENT	1 1.00
	1	(flip-flop\$1 or latch\$3))		
34	58		USPAT;	2004/01/15
		(reduc\$5 near3 current) and ((plurality	EPO; JPO;	14:26
		or multiple) adj3 (flip-flop\$1 or	DERWENT	
3.5		latch\$3))	ucpam.	2004/01/15
35	l '	(test\$3 adj2 IC\$2) and (reduc\$5 near3 current) and ((plurality or multiple)	USPAT; EPO; JPO;	14:26
		adj3 (flip-flop\$1 or latch\$3))	DERWENT	14.20
36	l 8	(test\$3 near2 IC\$2) and (reduc\$5 near3	USPAT;	2004/01/15
		current) and ((plurality or multiple)	EPO; JPO;	14:33
		adj3 (flip-flop\$1 or latch\$3))	DERWENT	
37	105	bernstein-k\$.in.	USPAT;	2004/01/15
			EPO; JPO; DERWENT	14:37
39	12	bernstein-k\$.in.and test\$3	USPAT;	2004/01/15
	13	DOLINGTON NY . III. AND CESSYS	EPO; JPO;	14:38
1			DERWENT	
38	3	bernstein-k\$.in.and stress\$3	USPAT;	2004/01/15
			EPO; JPO;	14:54
1.0	_	uppo and uppl and uppo	DERWENT	2004/01/15
40] 3	VDD0 and VDD1 and VDD2	USPAT; EPO; JPO;	2004/01/15 15:00
			DERWENT	13.00
41	14930	(first adj3 (latch or flip-flop)) same	USPAT;	2004/01/15
		(second adj3 (latch or flip-flop))	EPO; JPO;	15:01
			DERWENT	
42	1730		USPAT;	2004/01/15
		(second adj3 (latch or flip-flop))) and	EPO; JPO;	15:03
	!	((first adj2 logic) or (second adj3	DERWENT	
43	504	logic)) ((first adj3 (latch or flip-flop)) same	USPAT;	2004/01/15
33	1 304	(second adj3 (latch or flip-flop))) same	EPO; JPO;	15:03
		((first adj2 logic) or (second adj3	DERWENT	'
		logic))		
44	133		USPAT;	2004/01/15
		(second adj3 (latch or flip-flop))) same	EPO; JPO;	15:03
1		((first adj2 logic) or (second adj3 logic))) and test\$3	DERWENT	
		LOGIC and resits		!

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45	10	(((first adj3 (latch or flip-flop))	same	USPAT;	2004/01/15
	<u> </u>	(second adj3 (latch or flip-flop)))	same	EPO; JPO;	15:49
		((first adj2 logic) or (second adj3		DERWENT	
	1	logic))) and test\$3 and LSSD			
46	26	(((first adj3 (latch or flip-flop))	same	USPAT;	2004/01/15
		(second adj3 (latch or flip-flop)))	same	EPO; JPO;	15:04
		((first adj2 logic) or (second adj3		DERWENT	
		logic))) and (scan adj2 test\$3)			
47	12	(((first adj3 (latch or flip-flop))	same	USPAT;	2004/01/15
		(second adj3 (latch or flip-flop)))	same	EPO; JPO;	15:50
	•	((first adj2 logic) or (second adj3		DERWENT	
		logic))) and LSSD			